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# Bond strain and defects at Si–$SiO_2$ and internal dielectric interfaces in high-*k* gate stacks

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**Abstract**
The performance and reliability of aggressively-scaled field effect transistors are determined in large part by electronically-active defects and defect precursors at the Si–$SiO_2$ and internal $SiO_2$-high-*k* dielectric interfaces. A crucial aspect of reducing interfacial defects and defect precursors is associated with bond-strain-driven bonding interfacial self-organizations that take place during high temperature annealing in inert ambients. The interfacial self-organizations and intrinsic interface defects are addressed through an extension of bond constraint theory from bulk glasses to interfaces between non-crystalline $SiO_2$ and (i) crystalline Si, and (ii) non-crystalline and crystalline alternative gate dielectric materials.

## 1. Introduction

Two fundamental issues that impact on the introduction of deposited alternative high-*k* dielectrics into aggressively-scaled Si devices are addressed [1, 2]. The first derives from an interfacial transition region (ITR) between the $SiO_2$ buffer layer and the Si substrate, and the way in which this contributes to device performance and reliability after a 900 °C anneal or equivalent thermal exposure [3–5]. Previous studies demonstrated that replacement of thermally-grown $SiO_2$ dielectrics by deposited dielectrics, including $SiO_2$, as well as higher-*k* dielectrics, requires separate and independent steps for (i) formation of an ultra-thin, ∼0.5–0.6 nm $SiO_2$ buffer layer and its interface with Si, and (ii) deposition of the thin film dielectric [6]. The $SiO_2$ buffer layer and its ITR at the Si substrate contribute ∼0.35 nm to the equivalent oxide thickness (EOT) limiting the ultimate reductions of EOT to about 0.8 nm. The EOT is defined as the $SiO_2$ thickness corresponding to the entire gate stack, including the high-*k* alternative dielectric as well as an interfacial $SiO_2$ layer. The second issue deals with the conditions required for a second strain-driven bonding self-organization that is required to

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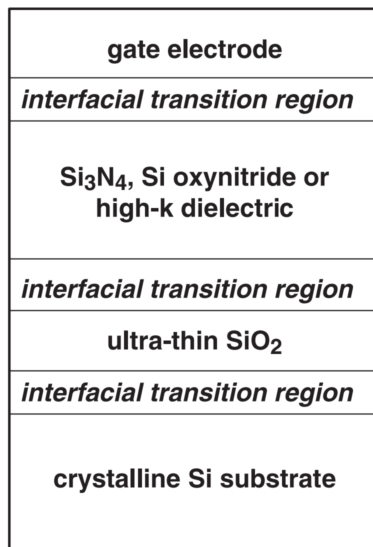



**Figure 1.** High-*k* gate with $SiO_2$ buffer layer.

reduce the fixed charge at the internal dielectric interface between the $SiO_2$ buffer layer and an alternative high-*k* gate dielectrics (see figure 1) [2, 7].

The $SiO_2$ interface with Si produced by thermal oxidation has been shown to be neither abrupt on an atomic scale, nor strain free [3–5]. Theoretical studies have found ITRs to be an intrinsic bonding property of these interfaces [8, 9]. A thin ITR with suboxide bonding provides a strain reducing buffer layer between the crystalline Si (c-Si) substrate, and the more *elastically compliant* non-crystalline $SiO_2$ dielectric film [10, 11]. Several factors contribute to interfacial bond-strain and subsequent formation of the ITR. Differences in the Si–Si interatomic distances in the c-Si substrate, 0.235 nm, and the $SiO_2$ dielectric, ~0.305 nm, generate intrinsic compressive stress in the oxide and tensile stress in the substrate [12].

Differences in linear thermal expansion coefficients between $SiO_2$ ($\sim 0.5 \times 10^{-6}$ $C^{-1}$) and the Si substrate ($\sim 2.5 \times 10^{-6}$ $C^{-1}$) contribute a component of thermal strain equivalent to several tenths of a per cent for oxides grown or processed at 800–1000 °C, and then returned to room temperature [12]. These levels of interfacial bond-strain cannot be relieved elastically and this pins a relatively high level of stress in the C–Si and the $SiO_2$ that define the interface, $\sim 5 \times 10^9$ dyn $cm^{-2}$.

These levels of interfacial stress can also result in *plastic deformation* with Si dangling bond formation in the $Si_D$ layer. Typical densities of dangling bonds as determined by electron spin resonance (ESR) are approximately $3\text{–}5 \times 10^{12}$ $cm^{-2}$ or on average about 0.3% of the Si atoms at the surface of a crystal oriented in the ⟨111⟩ or ⟨001⟩ directions [13, 14]. The symmetry of the *g*-tensor establishes that these dangling bonds reside in the Si substrate, and that the in-plane bonding of the Si atoms is locally in tensile stress at these defect sites.

Defect formation in the Si substrate and the internal dielectric interface is consistent with a novel application of bond constraint theory (BCT), originally proposed to account for the ease of glass formation in network solids such as $As_2S_3$ and $SiO_2$ [15, 16], but which is also applicable to semiconductor–dielectric and internal dielectric interfaces as well [17, 18].

Finally, single wavelength ellipsometry (SWE) studies were performed on Si–$SiO_2$ gate stacks grown by conventional thermal oxidation in dry $O_2$ at 850 °C and furnace annealed in

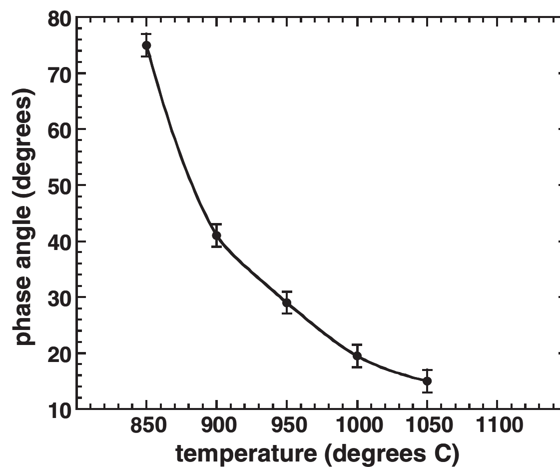



**Figure 2.** Second harmonic generation phase angle versus anneal temperature.

Ar up to 1100 °C [12]. These studies indicated a relaxation of intrinsic growth stress by a visco-elastic process at a temperature of ~980 °C.

## 2. Chemical bonding changes at Si–$SiO_2$ interfaces

### *2.1. Spectroscopic studies*

An interfacial relaxation has been identified from the optical second harmonic generation (SHG) response of a vicinal Si(111)–$SiO_2$ interface by studying the azimuthal anisotropy of the SHG signal, and extracting the temperature dependence of the phase angle, $\theta$, between terrace and step edge Fourier components of that signal [19–22]. The plot in figure 2 gives $\theta$ as a function of annealing temperature for an Si$\langle 111 \rangle$ interface with an off-cut angle of 5° in the $11\bar{2}$ direction. The largest change in $\theta$ is between 850 and 900 °C, and this has been interpreted as being due to bonding rearrangements on the terrace and step edges of the vicinal wafers [19–22]. It has also been addressed in the context of a bonding model [23].

Figure 3(a) summarizes results of soft x-ray photoelectron spectroscopy (SXPS) studies performed on Si$\langle 111 \rangle$ interfaces [11]. Spectral features identified as $I_1$, $I_2$ and $I_3$ correspond respectively to bonding groups in which Si has one, two and three oxygen neighbours, designated as $Si^{1+}$, $Si^{2+}$, and $Si^{3+}$ [5, 11]. The spectrum also includes the Si substrate feature, $S^0$, and the $SiO_2$ feature, $Si^{4+}$. The most significant change in the spectra after the 900 °C anneal is a marked reduction in the $Si^{2+}$ feature. A quantitative analysis of spectral changes in figure 3 indicates that after the 900 °C anneal there is one molecular layer of suboxide bonding with an average composition of SiO in excess of the one monolayer of $Si^{1+}$ bonding required at form an abrupt S$\langle 111 \rangle$–$SiO_2$ interface. This suboxide transition region corresponds to a physical thickness of ~0.3–0.4 nm [24], in good agreement with ion scattering measurements of [3], and the HRTEM studies of [10]. Similar bonding rearrangements between as-grown and 900 °C annealed spectra have been reported for Si$\langle 100 \rangle$–$SiO_2$–Si interfaces [11].

In the as-grown Si$\langle 111 \rangle$ interfaces, the bonding in the ITR with an SiO composition is approximately *random* with respect to the distribution of the $Si^{1+}$, $Si^{2+}$ and $Si^{3+}$ features, with a ratio close to 1:2:1. A random distribution must also include $Si^{4+}$ and $Si^0$ bonding arrangements; however, these cannot be distinguished from the respective $SiO_2$ and Si

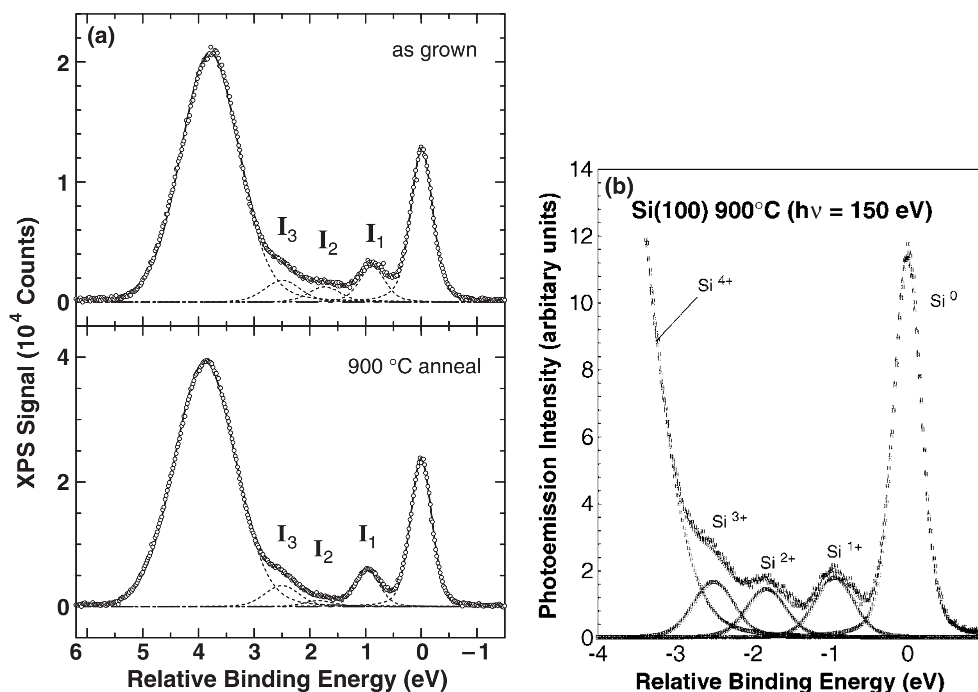



**Figure 3.** Soft x-ray photoelectron spectra for (a) the Si⟨111⟩ interface as grown, and after a 900 °C anneal, and (b) the Si⟨001⟩ interface after a 900 °C anneal.

substrate features. After the 900 °C anneal, the bonding in the ITR is no longer random, but instead consists primarily of $Si^{1+}$ and $Si^{3+}$ groups in a ratio of approximately 1:1, and with a significantly reduced $Si^{2+}$ component.

Figure 3(b) summarizes the results of SXPS studies performed on Si⟨100⟩ interfaces. After a 900 °C anneal this interface displays approximately equal intensities of $Si^{1+}$, $Si^{2+}$ and $Si^{3+}$ ITR features, each corresponding to approximately one monolayer of interfacial bonding. This means that there are approximately equal concentrations of $Si^{1+}$ and $Si^{3+}$ in addition to the one monolayer of $Si^{2+}$ required for a Si⟨100⟩ interface termination. The physical thickness of this ITR is also ~0.3–0.4 nm, in agreement with the results in [3, 10].

Cathodo-luminescence (CLS) results are shown in figure 4 for an Si–$SiO_2$ gate stack with an $SiO_2$ physical thickness of 5 nm [25]. Spectra were obtained as a function of the electron beam energy between 0.5 and 4.5 keV, with those in figure 4 at 2 keV revealing interface and near interface features. Spectra are shown for the as-deposited sample in which the interface was formed by 300 °C remote plasma-assisted oxidation (~0.6 nm) [6], and the $SiO_2$ layer by 300 °C remote plasma-enhanced chemical vapour deposition. Additional spectra are shown after (i) a 400 °C anneal in $H_2$, (ii) a 900 °C rapid thermal anneal (RTA) for approximately 1 min in Ar, and (iii) a 900 °C RTA followed by a 400 °C anneal in $H_2$.

The combination of an RTA at 900 °C and a 400 °C anneal in an H-containing ambient significantly reduces the interfacial CLS defect features. These are marked by arrows: DB, centred at about 0.9 eV, is an interfacial Si dangling bond; $D_1$, with a spectral peak at ~1.8 eV, is a near interfacial defect; and $D_2$, with a spectral peak at ~3.4 eV, is an Si substrate feature. The spectral peak and asymmetric line shape of the $D_1$ feature are essentially the same as a photoluminescence (PL) feature reported in [26] and [27] for an Si suboxide with $x \sim 1.1$.

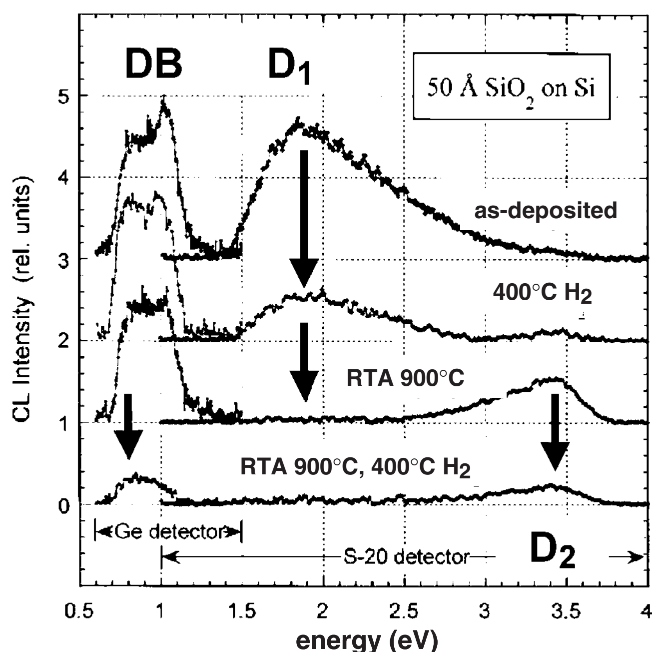



**Figure 4.** Cathodoluminescence spectra for a 5 nm $SiO_2$ gate stack.

The most significant changes after the 900 °C RTA and 400 °C $H_2$ anneal are the reduction of $D_1$ below the detection limit. The DB defect shows similar reductions to substrate Si-atom dangling bonds after a 400 °C $H_2$ anneal [13, 14]. These changes in DB luminescence establish that CLS is sensitive to defect changes at the $10^{11}$–$10^{12}$ defects cm$^{-2}$ regime.

## 2.2. *Kinetics of interfacial bonding changes*

A study of the stability of homogeneous bulk Si suboxide films deposited at 300 °C with compositions close to SiO, i.e., $SiO_x$, $x \sim 1$ [26], provides a basis for understanding bonding changes identified in the SXPS studies of Keister *et al* [11]. The studies of bulk $SiO_x$ films demonstrated a chemical phase separation into nano-crystalline Si (c-Si) and non-crystalline $SiO_2$ (nc-SiO) after isochronal annealing in the temperature range from 500 to 1000 °C. This is represented in equation (1) by following reaction:

$$SiO_x \rightarrow \text{c-Si} + \text{nc-}SiO_x, \qquad x \sim 1. \tag{1}$$

The kinetics of this bulk transition have been studied by FTIR to determine the *extent of reaction* as a function of annealing temperature [26], and they demonstrated that the reaction in equation (1) was ~90% complete after a 900 °C anneal in an inert ambient. The ITR chemical bonding changes from random to Si- and O-rich arrangements are qualitatively similar to those in equation (1).

Photoluminescence (PL) measurements on homogeneous $SiO_x$ films reinforce the interpretation of the CLS features in figure 3, in particular the assignment of the 1.8 eV CLS feature to defect bonding in the suboxide ITR. PL has been detected in homogeneous suboxide samples prepared by low temperature, 200–300 °C, plasma deposition processes [26, 27]. The spectral peak of CLS luminescence labelled $D_1$ in figure 4 is at approximately the same photon energy as the spectral peak of the $SiO_x$ feature in [27] for $x \sim 1.1$. Additionally, the studies

of [26] demonstrated that the same suboxide PL feature decreased significantly after annealing in inert ambients at temperatures between 650 and 750 °C, and was not detected after a 900 °C anneal.

### *2.3. Bond constraint theory and the $SiO_x$ bonding changes*

BCT provides a framework for describing the build-up of strain in network amorphous solids [17, 18]. BCT yields a linear relationship between the average number of bonds per atom, $N_{av}$, and the total number of valence bond-stretching and bond-bending constraints per atom, $C_{av}$, given by [15, 16]

$$C_{av} = 2.5N_{av} - 3. \tag{2}$$

The condition for an ideal strain-free CRN solid is that $C_{av}$ be equal to the network dimensionality of 3. This corresponds to a value of 2.4 for $N_{av}$, for the bonding constraints in equation (2).

BCT provides a remarkably accurate description of network stress in non-ideal continuous random network amorphous solids in which $C_{av} > 3$, including its consequences with respect to defect formation [17, 18]. This application of BCT is based on the simple idea that the valence forces in a network amorphous solid can be arranged in a hierarchy from stronger bond-stretching to weaker bond-bending forces. The constraining effects of these forces are a linear function of $N_{av}$ as in equation (2). For over-constrained networks such $SiO_x$ with $x \sim 1$ and $N_{av} \sim 3$, strain energy accumulates along bending constraints at the atom with the lower coordination, O. This means that Si–O–Si bond angles, $\theta$, are distorted from their average value, $\sim 150°$ [28, 29], by an amount $\delta\theta$, which is proportional to the difference between $N_{av}$ in this non-ideal strained network and $N^*_{av}$ in a strain-free network, e.g., $SiO_2$ in which a bonding constraint at the O-atom site is broken so that $N^*_{av} = 2.4$ [17, 18]:

$$\delta\theta \propto [N_{av} - N^*_{av}]. \tag{3}$$

It is further assumed that the bonding defects are broken bonds that relieve the build-up of local strain. The density of these defects is then proportional to the strain energy [17, 18], which is proportional to $[\delta\theta]^2$. The density of defects, $D$, then obeys the following scaling relationship:

$$D \propto [N_{av} - N^*_{av}]^2. \tag{4}$$

The interpretation of the bulk SiO results [26], combined with the CLS results, suggests that the changes in bonding at Si–$SiO_2$ interfaces after the 900 °C anneal in an inert ambient are also driven by a strain relief mechanism. In this model the interfacial defects in the defective region of the Si substrate, $Si_D$, act as nucleating centres for the ITR chemical separation into Si-rich and O-rich domains. In the defect nucleation model the scale for the nanoscale separation is then correlated with the density of Si dangling bonds in the substrate, $\sim 3 \times 10^{12}$ $cm^2$, or approximately 0.4% of the Si atoms on a $\langle 001 \rangle$ surface [13, 14]. Based on this model, the characteristic length scale, $r$, for interfacial chemical self-organization is estimated by setting

$$r \sim [d_{Si-Si}]_{Si(001)} \times [f_{db}]^{-0.5}, \tag{5}$$

where $[d_{Si-Si}]_{Si(001)}$ is the spacing between terminal Si atoms on a Si$\langle 001 \rangle$ surface, and $f_{db}$ is the fraction of Si-atom dangling bonds on that surface. This yields a characteristic length of ∼5 nm, which is shown to be consistent with interfacial roughness scattering in the channel transport of electrons and holes in FET devices as extracted from an analysis of carrier mobilities [30].

### *2.4. Self-organization transition at Si–SiO$_2$ interfaces*

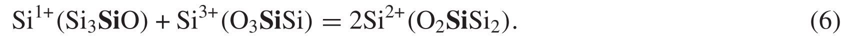
BCT has provided important insights into the physical mechanisms underlying (i) the formation of ITRs, and (ii) defect formation and defect relaxation at these interfaces [7]. The extension presented below builds on studies of Boolchand and co-workers on the nature of the glass transition, and the compositional dependence of the *floppy to rigidity* transitions that occur in glass forming binary alloy systems such as a-Se$_{1-x}$Ge$_x$ [31, 32].

Lucovsky, Phillips and co-workers have pointed out that Si–SiO$_2$ interfaces are heterostructures in which the substrate Si is effectively *rigid or over-constrained* with $N_{av}$ equaling exactly 4, and the SiO$_2$ dielectric is ideal or *elastically compliant* with an effective value of $N_{av} = 2.4$ [18, 33]. Since there is an ITR with bonding chemistry intermediate between Si and SiO$_2$ that separates these two regions of the gate stack, comparisons with a-Se$_{1-x}$Ge$_x$ chalcogenide alloys provide additional insights into the ITR properties [31, 32].

The ITR provides a continuous and smooth *transition* between tensile stress in the Si substrate and compressive stress in the SiO$_2$ dielectric. This suggests that the ITR plays essentially the same role as the *strain-free compositional regime* in the a-Se$_{1-x}$Ge$_x$ alloys. The bonding changes after the 900 °C anneal can then be construed as a strain-driven self-organization that prevents percolation of in-plane rigidity and thereby provides a low defect and defect precursor layer that bridges the Si substrate to the SiO$_2$ dielectric.

Consider first the ITR bonding for the Si⟨111⟩ interface in figure 3(a). The SiO bonding in excess of the one monolayer of $Si^{1+}$ required for an ideal abrupt Si⟨111⟩ interface termination in the as-grown ITR is random with the concentrations of $Si^{1+}$:$Si^{2+}$:$Si^{3+}$ having a ratio of approximately 1:2:1. After the 900 °C anneal, the excess ITR bonding is non-random with approximately equal concentrations of $Si^{1+}$ and $Si^{3+}$, and a significantly reduced concentration of $Si^{2+}$. The bonding in ITR for Si⟨100⟩ after the 900 °C anneal in figure 3(b) shows the same non-random bonding as the ITR for Si⟨111⟩, i.e., the bonding in excess of the one monolayer of $Si^{2+}$ is non-random with approximately equal concentrations of $Si^{1+}$ and $Si^{3+}$.

The bonding on average in the interfacial SiO regions for Si⟨111⟩ and Si⟨100⟩ as-grown, and after the 900 °C anneals is over-constrained with $N_{av} = 3.0$ and $C_{av} = 4.5$. The changes from random SiO bonding in as-grown interfaces to non-random bonding after the 900 °C anneals *mimic* those occurring in a-Se$_{1-x}$Ge$_x$ alloys for compositions between the onset of *local rigidity* and the percolation to a state of *global rigidity* [31, 32]. The local bonding in the SiO ITRs after the 900 °C anneal is equivalent to the average bonding in SiO as represented schematically in equation (6):



$$Si^{1+}(Si_3\mathbf{Si}O) + Si^{3+}(O_3\mathbf{Si}Si) = 2Si^{2+}(O_2\mathbf{Si}Si_2). \quad (6)$$

The terms in brackets identify the local tetrahedral bonding arrangements with respect to the central Si-atom that is listed second and highlighted in bold text. $N_{av} = 3.6$ for the $Si^{1+}$ groups and 2.8 for the $Si^{3+}$ groups corresponding to $C_{av}$ values of 6 and 4, respectively. However, discounting one bond-bending constraint per O-atom [15–18] reduces the respective values of $C_{av}$ to 5.8 and 3.5. There are additional reductions of $C_{av}$ associated with bending modes at the Si atom sites. These constraints are broken for bending vibrations whenever two end member atoms are different, as in Si–Si–O groups, in contrast with Si–Si–Si, and O–Si–O groups [33]. These *broken constraint* reduce $C_{av}$ to 5.4 for the $Si^{1+}$ cluster, and to 3 for the $Si^{3+}$ cluster. Non-random bonding after the 900 °C RTA can then encapsulate the Si-rich groups to prevent percolation of in-plane bond-strain. Strain-driven interfacial bonding-changes at Si–SiO$_2$ interfaces are effectively equivalent to the self-organization in the intermediate composition range of the Ge–Se alloys, so that the properties of these ITRs with respect to defects and defect formation are then expected to be similar to those associated with the intermediate state [31, 32].

Unlike the floppy and over-constrained Ge–Se alloy glasses and thin films which have high defects and defect precursors $>10^{12}$ cm$^{-2}$, those in the intermediate composition range have low defect concentrations $<10^{11}$ cm$^{-2}$, and do not age, showing reversible heat flow, and no changes in their glass transition temperatures with time [31, 32]. Similar defect properties have been found by CLS for the interfacial SiO transition regions, and these then impact significantly on device performance and reliability.

## 3. Internal dielectric interfaces

### *3.1. Fixed charge at internal dielectric interfaces*

Fixed charge has been reported at internal interfaces between $SiO_2$ and (i) $Si_3N_4$, (ii) an Si oxynitride alloy with a composition $(Si_3N_4)_{0.5}(SiO_2)_{0.5}$ [17], (iii) $Al_2O_3$ [34], (iv) Zr silicate alloys, $(ZrO_2)_x(SiO_2)_{1-x}$ [35], (v) Hf silicate alloys $(HfO_2)_x(SiO_2)_{1-x}$ [36], and (vi) Y silicate alloys $(Y_2O_3)_x(SiO_2)_{1-x}$ [37]. The fixed charge has been identified through capacitance–voltage, $C$–$V$ studies using standard analysis techniques on MOS capacitors with stacked dielectrics as shown in figure 1 [34]. The fixed charge is positive except for $Al_2O_3$ where it is negative. Fixed charge has been found in as-deposited Hf and Zr silicates, and it varies with Hf and Zr content from about $1 \times 10^{12}$ cm$^{-2}$ for alloys with $x \sim 0.25$ up to $\sim 4 \times 10^{12}$ cm$^{-2}$ for the end-member Hf and Zr oxides. Upon annealing to temperatures of ∼600–800 °C, the fixed charge is reduced by more than one order of magnitude [38, 39]. Additionally, high densities of negative charge, $\sim 10^{13}$ cm$^{-2}$, can be trapped at internal $SiO_2$ interfaces with $ZrO_2$ and $HfO_2$; these are due to processing in O-rich ambients, and are eliminated by annealing at ∼500 °C [40].

### *3.2. BCT and internal dielectric interfaces*

The density of defects, $D$, in a constrained network obeys the scaling relationship in equation (5), and similar scaling applies at internal dielectric interfaces including those between alternative high-$k$ dielectrics and $SiO_2$ [18]. The density of interfacial defects, $D_{\mathrm{int}}$, scales as the square of the *difference* in the $N_{\mathrm{av}}$ of the dielectrics, $A$ and $B$, that define the interface:

$$D_{\mathrm{int}} \propto [N_{\mathrm{av}}(A) - N_{\mathrm{av}}(B)]^2 = [\Delta(N_{\mathrm{av}})]^2. \quad (7)$$

This approach to scaling is analogous with the concept of heterovalency applied by Harrison *et al* to semiconductor $\langle 111 \rangle$ interfaces between Ge and GaAs, and GaAs and ZnSe [41]. At these lattice-matched interfaces, there is a significant mismatch between the number of electrons available for two-electron pair bond formation and the nuclear charge of the interfacial atoms. Electronically-active defects are formed by atomic rearrangements that provide charge balance at these heterovalent interfaces, paralleling defect formation in which there is a step in $N_{\mathrm{av}}$.

The plot in figure 5 applies the scaling relations of equation (7) for interfaces between $SiO_2$ and an Si oxynitride alloy, $Si_3N_4$, and several high-$k$ dielectrics, yielding a power law factor of $1.7 \pm 0.1$. This plot also includes the density of dangling bonds at the Si–$SiO_2$ interface, indicating that these defects have a similar origin to those at the internal dielectric interface. The value of $N_{\mathrm{av}}$ for $ZrO_2$ is based on an ideal eight-fold for oxygen, and the point for $Al_2O_3$ assumes that the interface bonding is associated primarily with six-fold coordinated $Al^{3+}$ ions. Finally a value of 2.67 has been used for $SiO_2$.

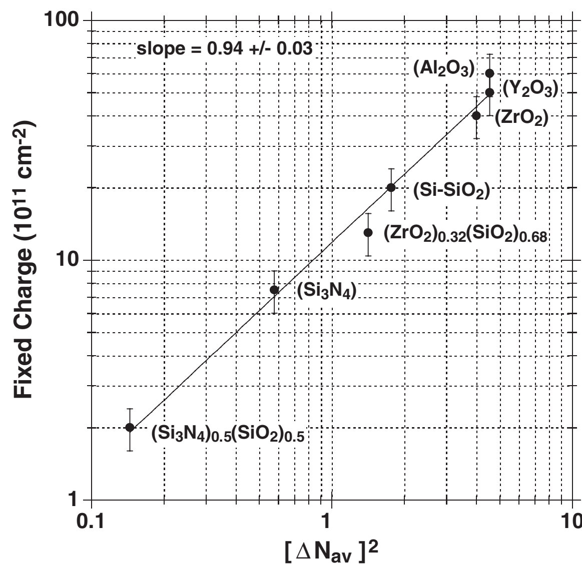



**Figure 5.** Defects versus $[\Delta N_{av}]^2$.

### 3.3. *Interfacial relaxation and phase diagrams*

A strain-induced self-organization occurs in the ITR at Si–$SiO_2$ interfaces during 900 °C annealing in inert ambients. Several conditions are necessary for the self-organization to take place: (i) the precursor bonding environments must be consistent with a bonding reorganization that reduces the total bond-strain rearrangements, and (ii) it must take place at temperatures consistent with the melting temperature of Si, the decomposition of $SiO_2$ at the Si–$SiO_2$ interface, and/or chemical and structural phase separation within the *bulk* dielectric film. It is equally important that there be no equilibrium phases with congruent melting points between Si and $SiO_2$, or between the end-member oxides at an interface between $SiO_2$ and a TM or RE oxide, silicate or aluminate high-*k* dielectric. The existence of such a phase would change the end-products in the chemical phase separation, and generally not result in a significant reduction in bond-strain energy, and/or impede the kinetics for the chemical phase separation and drive the effective temperature out of a range of annealing temperatures that meet other process integration restrictions.

All three relaxation conditions are met for Si–$SiO_2$ interfaces subjected to a 900 °C anneal [33]. The temperature of this relaxation is approximately 100 °C lower than the temperature for the onset of visco-elastic relaxation of growth-induced bulk film strain that involves the breaking of Si–O bonds in the bulk $SiO_2$ layer [12].

Interfaces between (i) $SiO_2$ and (ii) $Si_3N_4$ and Si oxynitride alloys display no evidence for a strain-driven self-organization after annealing and/or processing at temperatures up to more than 1000 °C. This is consistent with a compound phase, $Si_2ON_2$, between $SiO_2$ and $Si_3N_4$ with a congruent melting point in excess of 2250 °C [42]. However, the fixed charge at the $SiO_2$–Si oxynitride interface is sufficiently small that it does not degrade device performance and reliability in optimized MOS devices with $x \sim 0.5$ [17, 18].

Similar criteria also apply for interfacial chemical phase separation of TM and lanthanide RE silicate alloy thin films in contact with $SiO_2$. Those systems that do not have a compound phase with a congruent melting point have the potential to display a separation into the TM

or RE oxide, and $SiO_2$, whereas those that have a compound phase with a congruent melting point do not.

The equilibrium phase diagrams for $SiO_2$ and $ZrO_2$, and $SiO_2$ and $HfO_2$, have stable silicate phases but *without congruent melting points* at the respective silicate compound composition [43]. In addition, the liquidus curves display either *stable* or $O_2$ liquid immiscibility, and therefore are consistent with a spinoidal decomposition for silicate alloys formed by non-equilibrium thin film depositions. Thin film Zr and Hf silicate alloys respectively display a chemical phase separation into $SiO_2$ and $ZrO_2$, or $HfO_2$ at temperatures of at most 900–1000 °C [43, 44]. Based on the visco-elastic relaxation temperature of 1000 °C for bond-breaking in $SiO_2$, and the ITR self-organization at 900 °C, interfacial relaxations at Hf and Zr silicate or oxide interfaces with $SiO_2$ are expected to occur at temperatures lower than 800 °C. This has been realized in devices including Hf(Zr)$O_2$ and Hf(Zr) silicate alloys, where the fixed charge has been reduced by more than an order of magnitude for annealing temperatures about 600–800 °C [38, 39]. In contrast, devices with Zr and Hf silicate alloys annealed at 500 °C do not show fixed charge reductions [35, 36]. The reductions of [39] and [45] are attributed to an interfacial chemical phase separation into nanoscale crystalline $ZrO_2$ or $HfO_2$ encapsulated by $SiO_2$. This self-organization, like the separation of SiO into nanoscale c-Si encapsulated by $SiO_2$, also results in a decrease in interfacial bond-strain.

In contrast, and consistent with differences in equilibrium phase diagram between (i) $Al_2O_3$–$SiO_2$ [45], and (ii) $ZrO_2$–$SiO_2$ and $HfO_2$–$SiO_2$ [43], there is no reduction of defects at $SiO_2$–$Al_2O_3$ interfaces up to temperatures of at least 900 °C where the $Al_2O_3$ films undergo a bulk crystallization [34]. This is consistent with the existence of a compound composition with congruent melting point in excess of 1800 °C between $SiO_2$ and $Al_2O_3$ [45].

Compound phases with congruent melting points, such as $(Y_2O_3)_1(SiO_2)_2$ and $(Y_2O_3)_2(SiO_2)_1$, exist in the phase diagrams for the group IIIB TM metal atom silicates of Y and La, as well as the lanthanide RE elements in trivalent bonding states as well [43]. These effectively block self-organizations driven by bond-strain reduction, and account for levels of interfacial fixed charge, typically $>10^{12}$ cm$^{-2}$, even after annealing to temperatures of 900–1000 °C.

## 4. Discussion

This results presented in this paper have identified two strain-driven interfacial self-organizations that reduce defects and defect precursors at the Si–$SiO_2$ and internal dielectric interfaces in high-*k* gate stacks as represented schematically in figure 1. The self-organization at the Si–$SiO_2$ occurs at a temperature of approximately 900 °C, and changes the bonding in approximately one molecular layer with an average composition of SiO from a random distribution of local bonding groups to one with Si-rich and O-rich groups, reducing the relative concentration of $Si^{2+}$ arrangements at the expense of increases in Si-rich $Si^{1+}$ and O-rich $Si^{3+}$ arrangements. This bonding rearrangement is accompanied by the disappearance of an SiO defect luminescence band. Taken together, the change in bonding and reduction of defect luminescence are consistent with a description of the self-organization in the context of bond constraint theory. In this model, the self-organization is driven by bond-strain, and takes place at a temperature which is sufficiently high for changes in local bonding that require bonding-breaking and the transport required for the local rearrangements, in this instance ~900 °C. The self-organization establishes a defect/defect precursor ITR that bridges the tensile stress in the first few layers of the Si substrate, and compressive stress in the $SiO_2$ film that is on the other side of the ITR. The model further assumes that the nucleation sites for the chemical self-organization are the dangling bond sites of the Si substrate, which are produced by local

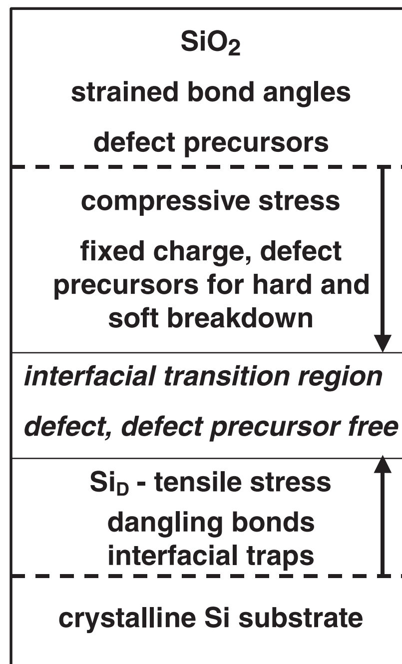



**Figure 6.** Defect profile for an Si–$SiO_2$ gate stack.

strain relief during oxide growth. These defects form to mitigate in part the in-plane strain associated with the molar volume mismatch between the Si substrate and the $SiO_2$ layer formed by a thermal or chemical oxidation process. Based on a dangling bond density of $3 \times 10^{12}$ cm$^{-2}$ from ESR, the characteristic distance between Si-rich regions is approximately 5 nm.

Figure 6 presents a schematic representation of the strain profile, defects, and defect precursors that are present in an Si–$SiO_2$ heterostructure that includes a strain-free, self-organized ITR in which the chemically-separated regions are in the nanometre size regime. Assuming that the nucleation of self-organized regions in the ITR is correlated with the density of dangling bonds in the tensile stressed Si substrate, this scale is estimated to be ~5 nm. This model is supported by the interface roughness parameter associated with the universality of the electron and hole channel mobilities in FETs [30]. The product of the correlation distance ($L$) and roughness 'height' ($H$) is ~0.2–0.3 nm$^2$. The difference in size or effective 'height' difference between Si-rich and O-rich bonding groups is ~0.05 nm, so that $L \sim 5$ nm, in good agreement with nucleation model of section 2.3.

Based on the ESR measurements of [13] and [14], the density of Si atom dangling bonds in the strained Si region $Si_D$ region is ~2–3 × $10^{12}$ cm$^{-2}$ for Si⟨100⟩ ($P_{b0}$ centres) and increases to ~5 × $10^{12}$ cm$^{-2}$ for Si⟨111⟩ ($P_b$ centres). There are additional $P_{b1}$ centres in the ITR for Si⟨001⟩ devices, and it is clear that these are present after a 900 °C anneal. These dangling bonds are H-atom terminated during a 400–450 °C post metallization anneal in an H-containing ambient such as forming gas. In MOS devices, H-atom release from these bonds has been proposed as a mechanism for defect generation during device operation [46].

The density of interface traps, $D_{it}$, has been studied as a function of annealing temperature at Si⟨111⟩–$SiO_2$ interfaces prepared by thermal oxidation at 850 °C, furnace annealed at temperatures up to 1100 °C for 30 min in Ar, and then subjected to a PMA for 30 min at

400 °C in forming gas after the initial growth and following each annealing step [18]. The most significant decreases in $D_{it}$ occur at a temperature of ∼980 °C, which is essentially the same as the onset of the release of growth induced stress [19]. In marked contrast, there is only a small decrease in $D_{it}$ after the 900 °C anneal, indicating that these defects are not reduced significantly by the atomic rearrangements that occur during the IRT self-organization. This difference is consistent with the $D_{it}$ defects being in the Si substrate in the immediate vicinity of the ITR.

These arguments, as well as defect modelling of hard and soft breakdown [47], lead us to conclude that (i) Si-atom dangling bonds and $D_{it}$ centres are located in the strained Si substrate region, $Si_D$, and (ii) the precursor states for soft and hard dielectric breakdown are in the compressive stress region of the $SiO_2$ film.

Finally, the inclusion of a high-*k* dielectric results in a second ITR between the $SiO_2$ buffer layer and the high-*k* dielectric. Fixed charge occurs at this interface as indicated above, but more importantly, the precursor centres for soft and hard breakdown reside primarily in the high-*k* part of the stack. In addition, electron trapping in the high-*k* part is generally greater than in $SiO_2$, and this becomes a significant issue for both performance and reliability.

Ultra-thin $SiO_2$ layers with self-organized ITRs play a key role in optimizing performance and reliability in CMOS devices that include alternative dielectrics. The addition of ∼0.35 nm to EOT from the $SiO_2$ buffer layer and the self-organized ITR place a significant constraint on ultimate EOT scaling, estimated by us to be at most 0.8 nm, rather than the 0.5 nm target of the ITRS [1].

Reduction of defects at internal dielectric interfaces is also crucial. The self-organization in ITRs at Si–$SiO_2$ interfaces is *a gift from nature*, and more importantly is consistent with the Si–$SiO_2$ binary phase diagram. The mismatch in interfacial $\Delta(N_{av})$ requires a similar self-organization at internal dielectric interfaces between $SiO_2$ and a high-*k* oxide or silicate. The conditions which permit self-organizations that reduce interfacial strain, reducing defects and defect precursors, have been correlated with equilibrium phase diagrams between $SiO_2$ and high-*k* TM and RE oxides. Based on this criterion only *two families* of high-*k* dielectrics will work. These are the oxides and pseudo-binary silicate alloys of Zr and Hf. Similar conclusions have been obtained by an analysis of direct tunnelling including the effects of d-states at conduction band edges [48].

Other factors related to device performance and process integration are equally important, and a complete discussion of these is outside the scope of this paper. These include (i) the electronic structure at the conduction band edge which is associated with localized d-states, rather than extended s-states as in $SiO_2$, which impact on band gaps, conduction band offset energies and the tunnelling mass of electrons [48], (ii) bulk traps associated with intrinsic aspects of high-*k* electronic structure [49], which determine charge injection and trapping that lead to the basis temperature instabilities (BTI) [50], as well as (iii) process integration issues including finding dual metal gate electrodes that match conduction band and valence band edges and are stable with respect to downstream processing.

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